## REMARKS

### I. Status of Claims

Claims 1-5 are currently pending. Claim 1 is amended. Claims 6-11 are proposed to be added. Therefore, upon entry of this Amendment, Claims 1-11 will be pending and under consideration for allowance. No new matter has been added by any of the claim amendments or the new claims.

### II. Specification

The Abstract of the disclosure stands objected to because there is more than one paragraph set forth therein. The Examiner states that it should be limited to a single paragraph. The Abstract has now been amended to include a single paragraph. The amendment does not add any new matter to the application. In light of the amendment, it is respectfully submitted that the objection to the Abstract should be withdrawn.

### III. Drawings

The drawings stand objected to under 37 CFR § 1.83(a) upon the basis that the drawings do not show every feature of the invention specified in the claims. Particularly, the Examiner states that the "inverter delay device" in Claim 3 must be shown or the feature canceled from the claims. Proposed amendments to Figures 1A and 1B adding the "inverter delay device" are indicated in red ink in the attached copy of Figures 1A and 1B. In the amendments, the block "INVERTER DELAY DEVICE", designated reference

numeral **8**, is included to show the inverter delay device recited in Claim 3. As shown, the block "INVERTER DELAY DEVICE" includes connections to gate **1** of transistor **2** and gate **2** of transistor **3**. Additionally, the paragraph beginning at page 6, line 33, of the specification has been amended to add reference numeral **8** corresponding to the "inverter delay device" in amended Figures 1A and 1B.

The proposed drawing amendment does not add any new matter to the application. Support for the proposed drawing amendment can be found on page 6, line 33, to page 7, line 13, of the specification. In light of the proposed amendments to Figures 1A and 1B and specification, it is respectfully submitted that the objection to the drawings should be withdrawn. Upon approval of the proposed drawing changes by the Examiner, applicant will submit new formal drawings for inspection and approval by the Official Draftsperson.

## IV. Claim Rejections Under 35 U.S.C. § 102

Claims 1, 4, and 5 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,160,417 to Taguchi (hereinafter, Taguchi). Applicant respectfully traverses the rejection and submits that the claims are allowable over the cited art for the following reasons.

It is well settled that for a cited reference to qualify as prior art under 35 U.S.C. §102, each element of the claimed invention must be disclosed within the reference. "It is axiomatic that for prior art to anticipate under 102 it has to meet every element of the claimed invention." Hybritech Inc. v. Monoclonal

Antibodies, Inc., 802 F.2d 1367, 231 U.S.P.Q. 81 (Fed. Cir. 1986). Thus, Taguchi must disclose each and every element of the claimed invention to be an anticipating reference under 35 U.S.C. §102(b). "Anticipation under §102 can be found only when the reference discloses exactly what is claimed and that where there are differences between the reference and the claim, the rejection must be based on §103 which takes differences into account." Titanium Metals Corp. v. Banner, 778 F.2d 775, 780, 227 U.S.P.Q. 773, 777 (Fed. Cir. 1985).

Upon careful consideration and review of Taguchi, applicant respectfully submits that Taguchi does not disclose each and every element of the presently claimed invention and therefore does not anticipate the presently claimed invention. Specifically, Taguchi does not disclose (1) an integrated circuit comprising a push-pull driving circuit having a first and second transistor including control terminals being controllably independent, load paths being arranged in series and between a first and second supply potential, and a centre tap forming a driving circuit connected with an output terminal of the integrated circuit; and (2) a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal.

Claims 4 and 5 depend from Claim 1. Therefore, Claims 4 and 5 include the limitations of Claim 1. Thus, the comments presented below relating to amended Claim 1 apply equally to Claims 4 and 5. To more particularly define and claim the subject matter of the present invention, Claim 1 is amended as indicated above to recite the following: (1) an integrated circuit comprising a push-pull driving circuit having a first and second transistor including control terminals being controllably independent, load paths being arranged in series and between a first and second supply potential, and a centre tap forming a driving circuit connected with an output terminal of the integrated circuit; and (2) a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal. Taguchi does not teach or suggest either of these elements. Support for these amendments can be found throughout the present patent application, notably in Figures 1A and 1B of the drawings.

The Examiner states that all of the features of Claims 1, 4, and 5 are taught by the system illustrated in Figure 3 of Taguchi. The system of Figure 3 discloses a system for transmitting a small-amplitude signal between a microprocessor **5** and a SDRAM **20** via a bus line **15**. Taguchi, column 1, lines

44-48. The system includes a push-pull-type output circuit **12** having a p-channel MOS transistor **13** functioning as a pull-up element and an n-channel MOS transistor **14** functioning as a push-down element. Taguchi, column 1, line 66, to column 2, line 2. As shown in Figure 3, transistors **13** and **14** are coupled in series between a line **26**, which supplies VCC power, and a line **27**, which supplies VSS power. Taguchi, column 2, lines 41-44. Microprocessor **5** includes an output terminal **6** connected to the coupling node of transistors **13** and **14** for connection to bus line **15**. Taguchi, Figure 3. Microprocessor **5** can transmit a low signal to SDRAM **20** by turning transistor **13** off and transistor **14** on. Taguchi, column 2, lines 22-27. Further, microprocessor **5** can transmit a high signal to SDRAM **20** by turning transistor **13** on and transistor **14** off. Taguchi, column 2, lines 27-29. Summarily, the system of Taguchi can transmit either a high or low signal on bus line **15** depending on the signal input into transistors **13** and **14**.

In contrast, the present invention, as claimed in amended Claim 1, applies only a single pulse on the output terminal in response to receiving both a positive and negative input pulse. The single input pulse is positive or negative depending on whether a single resistor, connected the output terminal, is of a pull-up or pull-down type. Thus, the output and input signals for the Taguchi system and the circuit of the presently claimed invention differ completely with regard to input and output. Therefore, Taguchi does not teach each and every limitation of the presently claimed invention and, thus, cannot anticipate the presently claimed invention.

Moreover, the resistors of the presently claimed invention provide an entirely different function than the resistors of the Taguchi system. Regarding Taguchi, the disclosed system includes termination resistors **28**, **29**, **30**, and **31**. Taguchi, column 2, lines 45-50. Taguchi discloses that resistors **28**, **29**, **30**, and **31** are set approximately equal to 50 or 100 ohms. Taguchi, column 2, lines 46, 47, and 51-54. Resistors **28** and **29** and resistors **30** and **31** are connected in series across supply voltages VCC and VSS. Resistors **28**, **29**, **30**, and **31** appear to perform the function of stabilizing the signal differences between lines **15**, **26**, and **27**. In contrast, the single resistor recited in Claim 1 of the present application can be selected to be either a pull-up or pull-down type for determining whether a single positive or a single negative control pulse is applied on the output terminal. The single positive or single negative control pulse is applied on the output terminal in response to the application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor. Thus, Taguchi does not teach each and every limitation of the presently claimed invention and, thus, cannot anticipate the presently claimed invention. For these reasons, it is respectfully submitted that the rejection of amended independent Claim 1 and dependent Claims 4 and 5 should now be withdrawn.

V. Claim Rejections Under 35 U.S.C. § 103

Claims 2 and 3 stand rejected as unpatentable over Taguchi in view of U.S. Patent No. 5,926,050 to Proebsting (hereinafter, Proebsting). This rejection is also respectfully traversed.

Applicant notes that the U.S. Court of Appeals for the Federal Circuit (C.A.F.C.) has set forth in Environmental Design Ltd. v. Union Oil Co., 713 F.2d 693 (Fed. Cir. 1983), cert. denied, 464 U.S. 1043 (1984), that the factual determinations to be made, as well as the evidence to consider, in making an obviousness determination under §103 include:

a) the scope and content of the prior art;

b) the differences between the prior art and the claimed invention;

c) the level of ordinary skill in the pertinent art; and

d) additional evidence, which may serve as indicia of non-obviousness.

All relevant evidence on each of these four dispositive issues must be fully considered and evaluated to determine whether the claimed invention would have been obvious. Additionally, it is well known that for an obviousness-type rejection to stand, the cited document or combination must disclose all aspects of the claimed invention; contain a suggestion to modify the cited document(s) to arrive at the claimed invention; and there must be a reasonable chance of success.

In Hodosh v. Block Drug Co., 786 F.2d 1136 (Fed. Cir. 1986), the U.S. Court of Appeals for the Federal Circuit set forth what is described as the

"tenets of patent law that must be adhered to when applying §103." Id. at 1143, n.5. Those tenets set out in Hodosh are:

a) the claimed invention must be considered as a whole;

b) the references must be considered as a whole and suggest the desirability and thus obviousness of making the combination;

c) the references must be reviewed without benefit of hindsight vision afforded by the claimed invention; and

d) "ought to be tried" is not the standard with which obviousness is determined.

Further, in Hartness International, Inc. v. Simplimatic Engineering Co., 2 USPQ2d 1826 (Fed. Cir. 1987), the U.S. Court of Appeals for the Federal circuit held that a dependent claim contains all of the limitations of the claim it depends upon plus a further limitation, therefore a dependent claim is not obvious if the claim it depends upon is not obvious.

Regarding Claim 2, the Examiner states that Taguchi teaches all of the features of Claim 2 except "disclosing a waiting time is provided between the first control pulse and the second control pulse, in which the two pulses do not overlap." Official Action, paragraph 6. The Examiner contends that Proebsting teaches the limitations not taught by Taguchi and that it would have been obvious to one of ordinary skill in the art to combine the teachings of Taguchi and Proebsting to arrive at the claimed invention. Official Action, paragraph 6.

Regarding Claim 3, the Examiner states: "Proebsting teaches in Figs. 4 and 5 the circuit of Claim 2, wherein one of the two control pulses (F2) is generated from the other of the two control pulses (C2) by an inverter delay device". Official Action, paragraph 6. Further, the Examiner contends that it

would have been obvious to one of ordinary skill in the art to combine the teachings of Proebsting and Taguchi to arrive at Claims 2 and 3.

Claims 2 and 3 depend from Claim 1. As stated above, Claim 1 has been amended to recite (1) an integrated circuit comprising a push-pull driving circuit having a first and second transistor including control terminals being controllably independent, load paths being arranged in series and between a first and second supply potential, and a centre tap forming a driving circuit connected with an output terminal of the integrated circuit; and (2) a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal. Summarily, neither Taguchi nor Proebsting, alone or in combination, discloses (1) an integrated circuit comprising a push-pull driving circuit having a first and second transistor including control terminals being controllably independent, load paths being arranged in series and between a first and second supply potential, and a centre tap forming a driving circuit connected with an output terminal of the integrated circuit; and (2) a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the

second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal.

As stated above, Taguchi does not disclose the above limitations of amended Claim 1. Proebsting fails to overcome the significant shortcomings of Taguchi. Proebsting is directed to a system for communicating the state transitions of a periodic digital signal from one circuit node to another with minimal delay. Proebsting, column 2, lines 17-20. Proebsting does not disclose (1) an integrated circuit comprising a push-pull driving circuit having a first and second transistor including control terminals being controllably independent, load paths being arranged in series and between a first and second supply potential, and a centre tap forming a driving circuit connected with an output terminal of the integrated circuit; and (2) a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal. Additionally, Proebsting offers no suggestion to modify the system disclosed therein to arrive at the presently claimed invention and,

consequently, the combination proposed by the Examiner does not offer a reasonable chance of success in combining the cited references.

As stated above, Claims 2 and 3 depend from claim 1. Therefore, the comments presented above relating to Claim 1 apply equally to Claims 2 and 3.

Applicant respectfully submits that the teachings of Taguchi and Proebsting cannot be combined to either teach or suggest each and every element of the present invention. Therefore, Claims 2 and 3 are believed to be patentably distinguished over the cited references. Applicant respectfully requests that the rejections of Claims 2 and 3 under 35 U.S.C. §103(a) be withdrawn and the claims allowed at this time.

## VI. Conclusions

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and such action is earnestly solicited.

Pursuant to 37 C.F.R. § 1.121, please find attached hereto a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version With Markings To Show Changes Made."** Deletions are indicated in brackets and additions are indicated in bold and underlining.

If any minor issues should remain outstanding after the Examiner has had an opportunity to study the Amendment and Remarks, it is respectfully requested that the Examiner telephone the undersigned attorney so that all

such matters may be resolved and the application placed in condition for allowance without the necessity for another Action and/or Amendment.

DEPOSIT ACCOUNT

The Commissioner is hereby authorized to charge the $110.00 surcharge fee for a One-Month Extension of Time to Deposit Account Number **50-0426**. The Commissioner is also hereby authorized to charge any deficiency or credit any overpayment associated with the filing of this correspondence to Deposit Account Number **50-0426**.

Respectfully submitted,

JENKINS & WILSON, P.A.

Date: 1-29-03 By: Richard E. Jenkins

Richard E. Jenkins
Registration No. 28,428

Suite 1400 University Tower
3100 Tower Boulevard
Durham, North Carolina 27707
Telephone: (919) 493-8000
Facsimile: (919) 419-0383

Customer No. Bar Code: 25297

1406/36 REJ/BJO

Version With Markings To Show Changes Made

IN THE SPECIFICATION:

The paragraph beginning at page 6, line 33, has been amended as follows:

-- Such a sequence of two successive control pulses A and B at the gates of the transistors 2 and 3 can be generated particularly simply by means of an inverter delay device 8 ( [not illustrated] shown in FIGs. 1A and 1B). In this case, the first control pulse A is generated from the second control pulse B by the second control pulse B being applied simultaneously both to the gate 2 and to [the] inverter delay device 8. If the edge rises at the gate G2, then it also rises at [the] inverter delay device 8. If the second control pulse B at the gate G2 falls again, the delayed and inverted rising edge is output as control pulse A to the first gate G1 by [the] inverter delay device 8. In this case, it goes without saying that the duration of the second control pulse B must be chosen such that the second control pulse B is returned to its original level again when [the] inverter delay device 8 outputs the first control pulse A. In order to reliably avoid a short circuit, in this case it is possible to provide a time interval between the two pulses A and B in which the two pulses A and B do not overlap. --

Please delete the phrase "Circuit for generating an asynchronous signal pulse" at page 10, line 2, of the Abstract.

Please delete the paragraph beginning at page 10, line 3, of the Abstract.

The paragraph beginning at page 10, line 5, has been amended as follows:

-- Circuit for Generating an Asynchronous Signal Pulse. The invention relates to a circuit for generating an asynchronous signal pulse in an integrated circuit. In order to generate a pulsed signal with a desired active state without a great outlay on circuitry, the circuit according to the invention is characterized by a first and a second transistor (2, 3) in the integrated circuit, which are connected in series between a supply potential ($U_{DD}$) and ground (GND), firstly a control pulse (A) having the predetermined duration being present at a control connection (G1) of the first transistor (2) and then a control pulse (B) being present at a control connection (G2) of the second transistor (3), with the result that, for the predetermined duration, firstly the first transistor (2) and then the second transistor (3) is turned on, and a resistor (6, 7) for the definition of the active signal state, which is connected outside the integrated circuit in parallel with one of the two transistors (2, 3) in the integrated circuit either between the supply potential ($U_{DD}$) and the connecting point (4) or between ground (GND) and the connecting point (4). --

Please delete the phrase "Figure 1a" at page 10, line 24, of the Abstract.

IN THE CLAIMS:

Please amend claim 1 as follows:

1. (Twice Amended) A circuit for generating [an] a single asynchronous signal pulse [having a predetermined duration] at

an output of an integrated circuit, [which has] the circuit comprising:

(a) an integrated circuit comprising a push-pull driving circuit having a first and second transistor including control terminals being controllably independent, load paths being arranged in series and between a first and second supply potential, and a centre tap connected with an output terminal of the integrated circuit; and

(b) a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal.

[a first and a second transistor in the integrated circuit, which are connected in series between a supply potential (UDD) and ground (GND), firstly a control pulse having the predetermined duration being present at a control connection of the first transistor and then a control pulse being present at a control connection of the second transistor, with the result that, for the predetermined duration, firstly the first transistor

and then the second transistor is turned on and the connecting point is firstly at the supply potential (UDD) and then at the ground (GND), and a resistor for the definition of the active signal state, which is connected outside the integrated circuit in parallel with one of the two transistors in the integrated circuit either between the supply potential (UDD) and the connecting point or between the ground (GND) and the connecting point.]

Please add the following new claims:

6. (New) A circuit for generating a negative signal pulse in response to receiving a sequence of a positive and negative control pulse, the circuit comprising:

   (a) a first transistor including a control terminal and a load path connected between an output terminal and a first supply potential for receiving a negative control pulse at the control terminal;

   (b) a second transistor including a control terminal and a load path connected between the output terminal and a second supply potential having a potential less than the first supply potential for receiving a positive control pulse at the control terminal in a sequence with the control terminal of the first transistor receiving the negative control pulse; and

(c) a pull-up resistor connected between the first supply potential and the output terminal for generating a negative signal pulse at the output terminal in response to the control terminals receiving the sequence of negative and positive control pulses.

7. (New) A circuit according to claim 6 wherein a waiting time is provided between the sequence of negative and positive control pulses such that the control pulses do not overlap.

8. (New) A circuit according to claim 6 further including an inverter delay device for generating one of the first and second control pulses from the other of the two control pulses.

9. (New) A circuit for generating a positive signal pulse in response to receiving a sequence of a positive and negative control pulse, the circuit comprising:

(a) a first transistor including a control terminal and a load path connected between an output terminal and a first supply potential for receiving a negative control pulse at the control terminal;

(b) a second transistor including a control terminal and a load path connected between the output terminal and a second supply potential having a potential less than the first supply potential for receiving a positive control pulse at the control

terminal in a sequence with the control terminal of the first transistor receiving the negative control pulse; and

(c) a pull-down resistor connected between the second supply potential and the output terminal for generating a positive signal pulse at the output terminal in response to the control terminals receiving the sequence of negative and positive control pulses.

10. (New) A circuit according to claim 9 wherein a waiting time is provided between the sequence of negative and positive control pulses such that the control pulses do not overlap.

11. (New) A circuit according to claim 9 further including an inverter delay device for generating one of the first and second control pulses from the other of the two control pulses.